CBCS SCHEME

USN | 4 | V | P | 2 | 0 | C | S | 0 | 3 | 4 | 18CS33

Third Semester B.E. Degree Examination, Feb./Mar. 2022
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What is biasing? Mention different BJT biasing techniques. Explain voltage divider bias. **(08 Marks)**

b. Explain relaxation oscillator. **(06 Marks)**

c. Write a note on opto coupler. **(06 Marks)**

OR

2 a. Explain active filters. List advantages of active filters over passive filters. **(06 Marks)**

b. Explain with diagram, R-2R ladder type D to A converter. **(08 Marks)**

c. Define op-amp. Explain the performance parameters of op-amp. **(06 Marks)**

Module-2

3 a. Explain Don't Care condition with an example. **(04 Marks)**

b. Reduce the following functions using K-map technique:
$F(P, Q, R, S) = \Sigma m(0, 1, 4, 8, 9, 10) + d(2, 11)$ **(08 Marks)**

c. Using Quine McClusky method, simplify the expression:
$F(P, Q, R, S) = \Sigma m(0, 3, 5, 6, 7, 11, 14)$
Write the gate diagram for the same. **(08 Marks)**

OR

4 a. Explain entered variable map method. **(05 Marks)**

b. Apply Quine McClusky method to find the essential prime implicants for the Boolean expression $f(a, b, c, d) = \Sigma m(1, 3, 6, 7, 9, 10, 12, 13, 14, 15)$ **(07 Marks)**

c. For the below expression, draw the logic diagram using AOI logic for minimal sum. Obtain minimal sum using K-map.
$F(a, b, c, d) = \Sigma m(1, 2, 3, 5, 6, 7, 11, 12, 13, 14, 15)$ **(08 Marks)**

Module-3

5 a. What is hazard? List the types of hazards. Explain static 0 and static 1 hazard. **(06 Marks)**

b. Differentiate between combinational and sequential circuit. **(06 Marks)**

c. Implement the following using PLA:
$A(x, y, z) = \Sigma m (1, 2, 4, 6)$
$B(x, y, z) = \Sigma m (0, 1, 6, 7)$
$C(x, y, z) = \Sigma m (2, 6)$ **(08 Marks)**

OR

6 a. Implement the following function using 8:1 multiplexer:
$f(a, b, c, d) = \Sigma m (0, 1, 5, 6, 8, 10, 12, 15)$ **(07 Marks)**

b. What is programmable logic array? How does PLA differ from PAL? **(06 Marks)**

c. Realize the following using 3:8 decoder:
(i) $f(a, b, c) = \Sigma m (1, 2, 3, 4)$ (ii) $f(a, b, c) = \Sigma m (3, 5, 7)$ **(07 Marks)**

Module-4

7 a. What are the three different models for writing a module body in VHDL? Give example for any one model. (06 Marks)
b. Derive characteristic equation for JK, T, D and SR flip flop. (08 Marks)
c. Give VHDL code for 4:1 multiplexer using conditional assign statement. (06 Marks)

OR

8 a. Using structural model, write VHDL code for Half Adder. (06 Marks)
b. Derive the excitation table for JK and SR flip flop. How SR flip flop is converted to T flip flop? (08 Marks)
c. With logic diagram, explain JK flip flop. (06 Marks)

Module-5

9 a. Define counter. Design synchronous counter for the sequence 0, 4, 1, 2, 6, 0, 4 using JK flip-flop. (08 Marks)
b. What is shift register? With a neat diagram, explain 4 bit parallel in serial out shift register. (08 Marks)
c. Write a note on sequential parity checker. (04 Marks)

OR

10 a. With a neat diagram, explain ring counter. (06 Marks)
b. Design and implement MOD 5 synchronous counter using JK flip-flop. Explain with timing diagram. (08 Marks)
c. Write a note on parallel adder with accumulator. (06 Marks)

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